REMARKS

In the Official Action, the Examiner rejected claims 1-30. Applicant respectfully requests reconsideration of the application in view of the remarks set forth below. Applicant believes that all pending claims are in condition for allowance, as summarized below.

First Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-15 under 35 U.S.C. § 102(e) as being anticipated by MacLaren (U.S. Patent No. 6,108,741). Applicant respectfully traverses these rejections.

A *prima facie* case of anticipation under 35 U.S.C. § 102 requires a showing that each limitation of a claim is found in a single reference, practice or device. *In re Donohue*, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985). Anticipation under 35 U.S.C. § 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under 35 U.S.C. § 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application is directed to a system and method for processing requests, according to an associated bus standard. The present system provides a way of efficiently processing transaction entries, even when they are received simultaneously. Entries are temporarily

stored such that they can be prioritized. Once the entries are prioritized according to a bus standard, they are selected from the temporary storage location and enqueued in a transaction order queue, according to the associated priority of each entry.

Specifically, independent claim 1 recites "prioritizing each of the plurality of temporarily stored transaction entries according to a bus standard," and "enqueuing the selected one of the plurality of temporarily stored transaction entries into... the transaction order queue according to an associated priority." Independent claim 6 recites "providing logic to prioritize each of the plurality of transaction entries according to a bus standard," and "providing a transaction order queue...configured to receive the selected one of the plurality of temporarily stored transaction entries according to an associated priority determined by the prioritization logic." Independent claim 9 recites "means for prioritizing each of the plurality of temporarily stored transaction entries according to a bus standard," and "means for enqueuing the selected one of the plurality of temporarily stored transaction entries into... the transaction order queue according to an associated priority determined by the prioritization means." Similarly, independent claim 12 recites "a temporary memory storage adapted to store a plurality of transaction entries" and "logic adapted for selecting and *ordering* the plurality of order transaction entries according to a bus standard."

Applicants respectfully submit that the MacLaren reference does not disclose prioritizing temporarily stored transaction entries according to a bus standard, such as PCI-X, selecting the entries based on priority, and enqueuing the entries from the temporary storage location into a transaction order queue according to the associated priority. Contrary to the Examiner's assertion, Applicant respectfully submits that the TRQ 2270 and TOQ 2272 disclosed in MacLaren cannot be fairly correlated with the features recited in the present claims. For instance, transactions in the TRQ 2270 are completed "in the order they were received." Col. 26, lines 63-65. Similarly, the

TOQ 2272 is a first-in-first-out (FIFO) queue. Col. 28, lines 34-36. Even assuming that the TRQ and the TOQ disclosed in the MacLaren reference could be fairly correlated with the temporary storage element and/or the transaction order queue recited in the present claims, it is clear that the MacLaren reference does not disclose "prioritizing each of the plurality of temporarily stored transaction entries according to a bus standard" and "enqueuing the selected noe of the plurality of temporarly stored transaction entries into... the transaction order queue according to an associated priority."

In general, MacLaren does not teach temporarily storing transaction entries, prioritizing those entries and then enqueuing the prioritized entries into a transaction order queue based on the priority, as recited in the present claims. In MacLaren, transactions are only sent to the TOQ 2272 if there is a posted memory write transaction in the TRQ 2270. "The TOQ 2272 is a first-in-first-out (FIFO) queue that retains the historical order of transaction received by the bridge after a posted memory write transaction is placed in the TRQ 2270." Col. 28, lines 34-37. "Because all transactions must wait for earlier-issued posted memory writes to run, all transactions including posted memory write, delayed request, and delayed completion transactions, are palced in the TOQ 227[2] (*sic*) when a posted memory write is enqueued in the TRQ 2270." Col. 28, lines 37-42. "Transactions in the TOQ 2272 must remain in the TOQ 2272 until the posted memory write transaction is removed from the TRQ 2270." Col. 28, lines 42-44.

In other words, even if the TRQ 2270 and TOQ 2272, could by hypothetically correlated with the temporary memory storage and the transaction order queue recited in the present claims, it is clear that in accordance with MacLaren, entries are *not* stored in the TRQ 2270, prioritized and then enqueued from the TRQ 2270 to the TOQ 2272. According to MacLaren, transactions are sent to the TRQ 2270, where they are processed in the order in which they are received. Col. 26,

lines 63-65. If a posted memory write is enqueued into the TRQ 2270, subsequent entries are *not* enqueued in the TRQ 2270, at all. Instead they are directed to the TOQ 2272 until the posted memory write is processed. Accordingly, entries are never stored in the TRQ 2270, prioritized and then moved from the TRQ 2270 to the TOQ 2272.

Accordingly, the MacLaren reference does not disclose each and every element recited in independent claims 1, 6, 9 and 12 or the subject matter of any claims dependent thereon. Because the MacLaren does not disclose each of the elements recited in independent claims 1, 6, 9, or 12, Applicant respectfully submits that these claims, as well as the claims dependent thereon, are not anticipated by the cited reference. Accordingly, Applicant respectfully requests withdraw of the Examiner's rejection and allowance of claims 1-15.

Second Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 16-19, 21-22, 24-26 and 28-29 under 35 U.S.C. § 102(e) as being anticipated by Olarig (U.S. Patent No. 6,175889). Applicant respectfully traverses these rejections. Applicant thanks the Examiner for indicating the allowability of the subject matter presented in claims 20, 23, 27 and 30. While Applicant agrees that these claims are allowable for the subject matter separately recited in each claim, Applicant has chosen not to amend the instant dependent claims at this time, as Applicant believes that the Olarig reference does not anticipate the subject matter recited in independent claims 16, 22, 25 and 28, as discussed further below.

Claims 16 has been amended to set forth the recited subject matter more clearly. Claim 16 recites, *inter alia*, a processing system comprising a first logic device, a second logic device, a third logic device, a plurality of registers and a transaction order queue. The

plurality of registers is "configured to receive a plurality of transaction entries from the first logic device." The second logic device is "adapted to receive the transaction entries from the plurality of registers and being programmed to *prioritize* transaction entries according to PCI-X specifications." Emphasis added. The third logic device is "adapted to select the transaction entries from the plurality of registers according to an associated priority," and "configured to enqueue the transaction entries into the transaction order queue according to the associated priority."

The Examiner cites the PCI-X bus Read/Write queues 402, 404 and 406 of Olarig as corresponding to the recited plurality of registers and cites the CPU Read/Write queues 420 as corresponding to the recited transaction order queue. The Examiner does not cite any elements corresponding to the recited logic devices, and does not address the respective functionality corresponding to the recited logic devices. The Examiner merely cites a passage in the Olarig that discloses general ordering rules for PCI-X transactions. Applicant respectfully submits that while Olarig may disclose PCI-X ordering rules, it does not disclose logic devices arranged in accordance with the system recited in claim 16. For instance, Olarig does not disclose a second logic device "adapted to receive the transaction entries from the plurality of registers and being programmed to *prioritize* transaction entries according to PCI-X specifications." Emphasis added. Therefore, the Olarig reference does not disclose or suggest that once the entries are stored in the PCI-X bus Read/Write queues 402, 404 and 406 (which the Examiner asserts corresponds to the recited plurality of registers), they are prioritized by a logic device. Further, the Olarig reference does not disclose or suggest a third logic device "adapted to select the transaction entries from the plurality of registers according to an associated priority," and "configured to enqueue the transaction entries into the transaction order queue according to the associated priority."

Accordingly, the Olarig reference does not disclose each and every element recited in independent claim 16 or the subject matter of any claims dependent thereon. Because the Olarig reference does not disclose each of the elements recited in independent claim 16, Applicant respectfully submits that claim 16, as well as the claims dependent thereon, are not anticipated by the cited reference. Accordingly, Applicant respectfully requests withdraw of the Examiner's rejection and allowance of claims 16-21.

Claim 22 recites a computer system comprising, *inter alia*, a transaction order queue "adapted to encode a plurality of simultaneously received transaction entries *according to an associated priority*, and comprising a transaction order queue comprising a plurality of storage locations, wherein each of the plurality of storage locations is configured to *store* one of the transactions from the memory device, *in an order according to the associated priority*." Emphasis added. Similarly, claim 25 recites "temporarily storing a plurality of simultaneously received transaction entries," and "delivering the plurality of transaction entries to a transaction order queue one at a time, wherein each of the plurality of transaction entries is *stored* in a respective one of a plurality of storage locations in the transaction order queue, *in an order according to an associated priority*." Emphasis added. Claim 28 recites, "temporarily storing a plurality of simultaneously received transaction entries," "*prioritizing* each of the temporarily stored transaction entries," and "*transmitting* the stored transaction entries to the transaction order queue *according to priority*, wherein each of the stored transaction entries is transmitted to a respective one of a plurality of storage locations in the transaction order queue." Emphasis added.

As discussed above, Applicant respectfully submits that Olarig does not disclose storing, selecting, encoding or transmitting transaction entries from one storage location to another storage location according to priority, before the requests are processed. Accordingly, the the Olarig reference does not disclose each and every element recited in independent claims 22, 25 or 28 or the subject matter of any claims dependent thereon. Because the Olarig reference does not disclose each of the elements recited in independent claims 22, 25 or 28, Applicant respectfully submits that claims 22, 25 and 28, as well as the claims dependent thereon, are not anticipated by the cited reference. Accordingly, Applicant respectfully requests withdraw of the Examiner's rejection and allowance of claims 22-30.

Conclusion

In view of the remarks and amendments set forth above, Applicant respectfully requests allowance of the pending claims 1-30. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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